CONTRIBUTED PAPER

RFID: From Supply Chains to Sensor Nets

A programmable wireless identification and sensing device is powered through energy harvesting and a software-defined RFID reader provides the means to investigate optimization approaches for RFID systems.

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ABSTRACT | The next generation internet will be the internet of things (and not just of computing devices like PCs, PDAs); this is presumed to be enabled by integrating simple computing plus communications capabilities into common objects of everyday use. Radio-frequency identification (RFID) is a compelling technology for creation of such pervasive sensor networks due to its potential for ubiquitous, low-cost/low-maintenance use. However, the current drivers for RFID deployment emphasize supply chain management using passive tags, implying that RFID sensor nets require advances beyond the components and system designs aimed at supply chain applications. This work provides a glimpse of how this may be achieved.

KEYWORDS | Backscatter modulation; link and MAC optimization; low-power wireless sensing; RFID; sensor nets

I. INTRODUCTION AND CONTEXT

Radio-frequency identification (RFID) was intended as a new generation technology to supplant or complement optical bar code scanning of tagged objects. As such, their primary application was anticipated to be in retail point-of-sale scenarios (where optical scanning is pervasive) as well as enabling newer applications within the supply chain, particularly for more effective inventory management and improved process reliability by eliminating human errors. However, RFID deployment in supply chains was predicated on *very low-cost*, *passive* tags that support reliable, speedy reading of tag IDs. Even in controlled environments, this proved to be a greater technical challenge initially than the anticipated "promise" of RFID in popular media. The maturation of RFID components and technology over time has yielded some large deployments recently; see, for example, [5] about item level tagging by the German retailer METRO. Undoubtedly, the advent of a new Class 1 Gen 2 RFID standard [2] has contributed significantly to these goals compared to the legacy Gen 1 standard [1], and consequently spurred other potential applications of RFID such as vehicle ID/tolling and secure access control as in keycards or passports. In other words, we are at a cusp of a virtuous cycle for RFID technology in nonsupply chain scenarios—notably those supporting notions of ubiquitous computing that are fundamentally based on interactions between a large number of tagged objects.

The internet of things translates to an environment of everyday networked objects that are sensor enabled, and can undertake communications/control/decision actions to create smart spaces. The potential attractiveness of RFID in enabling such a vision is largely based on the *key* advantages of RFID components relative to other technologies: small form-factor tags (that make it truly ubiquitous) that afford the potential for longer life, resulting from optimized low power operations and energy harvesting.

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We seek to highlight our work aimed at enhancing Gen 2 standard compliant RFID components towards the goal of RFID-based sensor networking. This immediately confronts current architectural assumptions underlying RFID system concepts that are strongly *asymmetric* by design and exclusively serve one-way, low-rate traffic (uplink, tag to reader communication of short messages comprising tag ID) and were never intended for streaming sensor data. New RFID sensor net designs must look to overcome this noncollaborative asymmetry at the link level—little functionality and processing power at the tag and all processing at the reader—that imposes significant constraints on achievable system performance. For example, the anticipated higher data rates for sensor nets will exacerbate *tag collisions* on the uplink with existing protocols; future RFID networks are thus likely to be uplink limited, based on this consideration. On the other hand, as deployments scale to larger tag populations requiring in turn many more readers in a given area, the likelihood of reader collisions (inability by tags to decode reader commands) on the downlink will also increase (for a given frequency band or number of channels). Translated into priorities for research at the component and network level design principles, these indicate the need for:

1) more efficient RFID tag front-end and mixed-signal designs (particularly *vis-a-vis* novel power harvesting approaches) as well novel sensor integration techniques;
2) enhancement to Gen 2 link layer design (particularly, modulation and coding) as well as receiver signal processing to improve link robustness;
3) enhancements to Gen 2 MAC protocols to achieve both *increased utilization* as well as *power efficiency* suitable for dense deployment scenarios with higher aggregate throughput.

A. RFID System Overview and Design Objectives

The two key RFID subsystems are the 1) readers/interrogators and 2) tags/transponders (the latter are affixed/associated with the object which is to be identified). The tag is composed of an antenna and an integrated circuit (IC) with the following functionalities: power rectification, clock, modulation and demodulation, memory.[1] RFID systems worldwide may operate over a wide variety of frequency bands, e.g., 125 kHz, 13.56/433/900 MHz, 2.45/5.8 GHz. In our work, we will exclusively focus on systems operating in the 900-MHz band based on electromagnetic radiated coupling.

The Gen 2 standard [2] defines communication between RFID readers and passive RFID tags in the 900-MHz band. The communication between the RFID reader and tags is reader initiated (reader talks first) as determined by current Gen2 communication protocols; the reader sends out a query (downlink) asking for a subset of the tags in its interrogation domain to respond with their IDs (uplink). For the uplink (assuming that the tag IC remains powered), the tag alters the reflection coefficient by varying the IC input impedance so as to enable *backscatter modulation* of the incident radiation of the readers CW signal. A typical RFID deployment consists of a network of readers and associated tagged objects that lie within the *uplink range* (of potentially multiple readers)—defined as the maximum distance at which the RFID reader can decode the backscattered signal from the tag.

[1]Typically, current tags include *no sensing* capabilities, a necessary feature for future sensor-net applications.

II. COMPONENTS AND FUNCTIONALITIES

RFID passive tags consist of the following key components: 1) the RF front end including the antenna, 2) the analog circuity for voltage multiplication and rectification, and 3) a (low power) digital back end. The radio-frequency (RF) voltage developed at the tag antenna during the period when an unmodulated carrier is sent on the downlink is converted to direct current (dc) by employing a voltage multiplier and regulator circuitry at the tag IC front end [6]. Clearly a number of design choices—affecting tag power consumption and storage and the hardware/software implementations on the IC—have significant impact on overall system performance.

Tags may be classified as 1) passive, 2) active, and 3) semiactive/passive. While an active tag has its own battery that is used for all operations, a passive tag is powered solely by radiated energy from an external source (either intentional or by opportunistic scavenging). The semipassive tag has its own battery, however it is only used to power the IC operations and not for uplink communications. Generally, active or semipassive RFID tags have much longer operating range than the passive tags, and expectedly, longer lifetimes. The absence of a power supply makes passive tags much cheaper as they consist of a single ASIC other than the antenna circuitry. Commercial implementations require less than 1 mm^2 for the IC, or several squared centimeters for PCB implementations with COTS components, facilitating item-level tagging or applications where small form factor is paramount. The inclusion of a battery typically necessitates a larger, PCB-based platform. In principle, the active tag circuitry could be integrated onto a single ASIC; however, high ASIC cost and the availability of high-performance COTS components have resulted in much less interest in active tag ASICs.

For active tags, the network lifetime T corresponding to battery capacity of E_{batt} Joules can be estimated according to the relation: $P_{\text{leak}} * T + N * E_{\text{task}} = E_{\text{batt}}$, where P_{leak} is the quiescent leakage power, and N is the number of tasks performed with E_{task} expenditure of energy per task. Accordingly, increasing node lifetime is accomplished by a low duty cycle and optimization for low P_{leak}.

A. Tag RF Front End and Analog Circuitry

Given form-factor limitations and the need for efficient power harvesting, innovative antenna designs for passive tags [8] is an area of ongoing innovations. We will limit our observations in this regard by noting that the dipole and its derivatives are the common templates for tag antennas [3]. Known disadvantages of a typical half-wave dipoles—length of 16 cm at 915 MHz and small reactance compared to that of the tag IC input impedance and lack of conjugate matching—has lead to *meandered dipole* designs [8]. With sufficient number of bends, the dipole can be made much shorter for the same length of wire, achieving lower inductance and capacitance per unit area [3]. Other contending designs such as *dual dipoles* have also been employed since tags may assume arbitrary orientations in the field of the reader antenna; the resulting polarization mismatch between reader and tag antennas leads to significantly reduced power transfer. However, such dual dipoles require dual rectifiers and dual bond pads, increasing tag complexity and reducing yield.

One of the other important considerations is the *minimum* voltage needed to power the on-tag chip reliably. Traditionally, an N-stage voltage multiplier circuit (such as a Dickson multiplier) is inserted between the RF front end and the tag IC, with N chosen to satisfy the minimum required voltage. Historically, Schottky diodes have been used in the multiplier circuit to utilize their very low turn-on voltages, low series resistance, and low junction capacitance; however, ultralow cost tags demand low-cost complementary metal–oxide–semiconductor (CMOS) processes. The design parameters involve the number of stages of the voltage multiplier, the size of the diodes, and the coupling capacitors. The main constituent of the IC input impedance arises from the voltage multiplier circuit—a parallel of a resistance and a capacitance. The capacitive term arises from the many contributing diode capacitances of the on-chip multiplier; however, the real part is generally much smaller in magnitude than the imaginary part with careful design. Thus, the input stage of the tag IC is a high Q network[2] that forces stringent constraints on the antenna design for conjugate matching.

B. Tag Power Consumption Models

Different types of tags (active, passive, semipassive) have radically different power models. For active tags, the network lifetime T corresponding to battery capacity of E_{batt} Joules can be estimated according to the relation: $P_{\text{leak}} * T + N * E_{\text{task}} = E_{\text{batt}}$, where P_{leak} is the quiescent leakage power, and N is the number of tasks performed with E_{task} expenditure of energy per task. Accordingly, increasing node lifetime is accomplished by a low duty cycle and optimization for low P_{leak}.

[2]As is usual, the quality factor Q is the ratio of the imaginary part to the real part of impedance.

Conventional passive tags implemented as an integrated circuit plus antenna have very little energy storage (typically capacitive) capability, effectively limiting the tag instantaneous power consumption P_{task} to the average power received. P_{task} comprises analog biasing, regulation and demodulation circuitry as well as digital logic. The switching power consumption component of the digital logic can be estimated by $P_{sw} = \alpha V_{dd}^2 f_{clk} C_L$ where the switching activity α, supply voltage V_{dd}, and design complexity factor C_L are determined by the IC technology and protocol complexity. The clock rate f_{clk} of the processor is the desired (maximum) rate of execution corresponding to the link and MAC processing. Generally speaking, this must be supplied by the averaged received power obtained from the reader. The Friis formula for the radiated power impinging on the tag $P_{rx,\text{Friis}} = P_{tx}\ G_{tx}\ G_{rx}(\lambda/4\pi r)^2$ where r is the separation distance, P_{tx} is the reader transmit power [Federal Communications Commission (FCC) limit of 30 dBm], and reader and tag antenna gains G_{tx}, G_{rx} are 6 and 2 dBi, respectively. Assuming tag rectifier efficiency of 15%, the power available at 1(10) m is 640(6.4) μW; tags currently need around 12–40 μW of power during the read cycle [3].

The communication throughput of passive tags is limited by different mechanisms depending on the wireless range. At close distances where $P_{rx,\text{Friis}} > P_{\text{task}}$, the throughput is protocol limited. The tag has sufficient power to process all communications, and the reader operates at allowable rates in the EPC Class 1 Gen 2 standard. At longer distances where $P_{rx,\text{Friis}} < P_{\text{task}}$, a passive tag can no longer operate. However, given an energy storage mechanism, the tag can duty cycle with fraction η in order to achieve $P_{av} = (P_{\text{task}}/\eta) \geq P_{rx,\text{Friis}}$. This duty cycling reduces the average data rate so as to meet the constraint $E_{\text{task}} = V_{dd} I_{\text{task}} T_{\text{task}} < E_{\text{stored}}$ where E_{stored} is the usable energy stored in the capacitor. The usable stored energy in the capacitor C is $E_{\text{stored}} = (1/2)C(V_{\text{tag}}^2 - V_{dd}^2)$ where V_{tag} is the tag rectifier output voltage and V_{dd} is the minimum operating voltage of the tag IC. Since $E_{\text{stored}} \geq E_{\text{task}}$, the minimum voltage required on the tag is $V_{\text{tag,min}} = \sqrt{(2E_{\text{task}}/C) + V_{dd}^2}$.

The E_{task} and $V_{\text{tag,min}}$ for several common tasks are listed in Table 1 using the wireless identification and sensing platform (WISP) [12] as a case study, for which $V_{dd} = 1.8$ V and $C = 10$ μF. Finally, the tag becomes ineffective when RF-to-dc conversion inefficiencies prevent generation of sufficient voltage V_{gen} to operate the tag V_{tag}, as summarized in Table 2.

Table 1 E_{task} for Various Cases

Task Description	T_{task}	I_{task}	E_{task}	$V_{tag,min}$
Transmit ID	6.75 ms	550μs	10.8μJ	2.14 V
Sense Temp.	50μs	50μs	0.9nJ	1.8 V
Sense Acceleration	5 ms	180μs	1.62μJ	1.89 V

Table 2 Tag Operating Regimes

Region	Near	Far	Out of Range
Definition	$P_{rx} > P_{task}$	$P_{rx} < P_{task}$	$V_{gen} < V_{tag}$
Constraints		$P_{tag} \leq P_{rx}$; $E_{task} \leq E_{stored}$	Insuff. voltage
Commn. Rate	Protocol limited	Power limited	Voltage limited
Duty Cycle	100%	P_{rx}/P_{task}	0%
Compatible Implementns.	Storage Cap/ No Cap	Storage Cap	No passive soln.

The energy required to complete a task E_{task} is strongly dependent upon the circuit implementation. The cost of improved efficiency is reduced configurability; a general purpose microcontroller can execute arbitrary instructions while the ASIC design is generally limited to configuration settings. The well-documented flexibility/power tradeoff in digital design is particularly acute in passive RFID applications as shown in Table 3; note that the power dissipation ranges over one order of magnitude.

In Table 3, note that the clock rate for the microcontroller is double that of the complex programmable logic device (CPLD) and ASIC implementations. The sequential nature of instruction processing in the microcontroller causes significant inefficiency; in [7], only a subset of the slower Gen2 modulation rates are possible with this clock rate. The CPLD and ASIC, however, can achieve all of the Gen2 modulation rates, as an example of the tradeoff between flexibility and performance.

Fig. 1 presents an operational duty cycle (the fraction of queries that the tag responds to)—for example, if communication with a tag requires 10 ms, 100% duty cycle represents the maximum rate of 100 Hz. To a first order, as long as the energy constraint is met (i.e., the tag stores enough energy to communicate once), the protocol rate does not affect the duty cycle. As the protocol rate is increased, the communication energy required is approximately constant. Assume that the tag must operate at a clock frequency equal to the protocol bit rate. Then, for digital switching power P_{sw}, the energy required to transmit N_{bits} is $E_{\text{task}} = (N_{\text{bits}} P_{sw}/f_{clk}) = \alpha N_{\text{bits}} C_L V_{dd}^2$.

The load capacitance C_L and activity factor α are related to the protocol complexity and the tag configurability, and is reflected in Table 3 data, where the total energy consumed is designed to be independent of the protocol rate. Thus, to achieve high throughput at longer distances, designs must push the limits of IC technology to reduce V_{dd} and minimize transistor count C_L through custom ASIC design and reduce switching through design optimization. High-performance sensor tags will thus favor conventional IC design for high throughput, small size, and low cost. However, several motivations remain for a tag that includes an energy storage mechanism since it is unclear whether sensors will benefit from IC scaling.

Table 3 Power Consumption

Implementation	Power @ min f_{clk}	Configurability	Cost
TI MSP430F2132	1.5 mW	High	$ 100
Xilinx CoolRunner X256 CPLD	130 μW	Medium	$ 100
Impinj Monza Gen2 Tag	8 μW	Low	$0.10 (bulk)

C. Backscatter Modulation and Link Budget

RFID tags backscatter part of the incident wave from the reader for uplink communication. Modulation of the backscattered wave is achieved by altering the input impedance of the tag IC between two different states [6]. Since the input impedance of the tag IC is complex, two options exists—modulate the real part (R_{LOAD}) for amplitude shift keying (ASK) or modulate the imaginary part (C_{IC}) for phase shift keying (PSK). The very nature of backscatter implies that a tradeoff exists between power transferred to the tag and the backscattered component. Of the two states of IC's input impedance, one corresponds to conjugate match for maximum power transfer to tag IC (hence, minimum backscatter). The other state then serves to maximize backscatter via modulation of the real or imaginary part of the chip complex impedance corresponding to ASK or PSK. The use of backscatter on the uplink implies that the modulation switching need only operate at a few kilohertz (regardless of the reflected signal

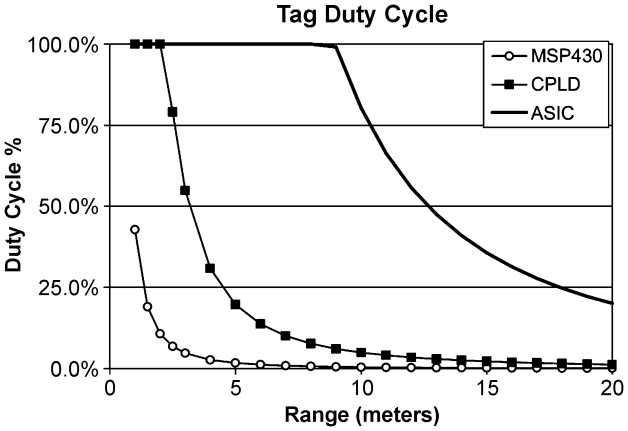

Fig. 1. *Tag duty cycle as a function of range and implementation.*

at 900 MHz) [3], saving tag power consumption; it also greatly simplifies tag design as no local oscillator is required.

Passive-tag-based RFID systems are (strongly) power limited and depend on rectification of downlink signal from the reader to operate the tag circuitry. The availability of sufficient power at requisite voltage for tag IC operation is the system limiter, as opposed to tag receiver sensitivity (minimum received signal level at which the tag can reliably *decode* the downlink signal); i.e., passive tag systems are downlink (range) limited [3]. On the other hand, operation of battery-assisted tags [3], with a power source such as a coin cell, are not limited by tag power considerations. Instead, such semipassive (or active) tags are uplink limited by the reader sensitivity, or equivalently, by the backscattered received power at the reader. The above highlights an important facet of RFID systems—the fundamental *asymmetry* of the uplink and downlink ranges at which (two-way) information may be reliably communicated. With continuing advancements in IC technology, RFID tags that consume much less power than their predecessors [6], [9] are being designed, which directly contributes to this. For example, Curty *et al.* [13] proposed a novel RFID tag that consumes only 2.7 μW, significantly lower than the 16.7 μW in [6].

The above points to several potential degrees of freedom for optimizing the uplink range in future RFID systems. For starters, more advanced modulation schemes beyond the binary—notably ASK and PSK and combinations—that are consistent with RFID tag technology evolution will be feasible. Each modulation will be characterized by a modulation index that, in turn, determines the power backscattered to the reader. Our recent work [10] demonstrates that judicious choice of the IC impedance for backscatter modulation may be used to simultaneously maximize uplink and downlink ranges as a function of improving tag receiver sensitivities. Further, more sophisticated coding approaches (e.g., coded modulation) beyond those specified in the Gen2 standard will likely be considered. In summary, more sophisticated link and multiple access designs will be a key enabler of RFID sensor nets, and this is explored further in the next section.

D. Gen2 Link and MAC Layers: Uplink

Via a downlink command, the reader sets up various uplink parameters—frequency, encoding (FM0 or Miller), etc. In all cases, the rate of ASK or PSK backscatter modulation is varied according to the data encoding, implying that the received signal at the reader is frequency shifted with respect to the CW downlink. This is necessary because reader transceiver architectures are half-duplex; accordingly, the desired weaker uplink (backscattered) signal must be protected from any leakage from the higher power CW downlink (which stays on during uplink receive); the greater the separation, the more effective the potential isolation. Thus, in FM0 encoding, "0" may appear as a frequency offset of 100 KHz and "1" of 200 KHz, respectively. The Miller encodings (or subcarrier modulation) are more robust to error as they allow greater separation but have a lower data rate (more symbols per bit), which can range from 5 to 640 kb/s. In general, increasing the data rate of the tag signal spreads out the received signal in frequency; while this is effective for providing isolation between uplinks and downlinks, it also leads to more bandwidth inefficiency, as channels used by neighboring readers must now be further separated to reduce interference. Clearly, there is a tradeoff between ensuring reliability of a single uplink versus reduced bandwidth efficiency of the network. However, uplink benefits may also derive from other dimensions, notably advanced PLL design techniques at the reader that concentrate on improving the phase noise characteristic, which constitutes the performance limiter on the uplink signal, due to the aforementioned transmit signal leakage into the receive path.

Broadly, RFID network architecture is "cellular" in nature, whereby (overlapping) cells are distinguished by some form of frequency planning (as in frequency hopping) for interference avoidance. The reader acts as a controller for the uplink tag responses, i.e., the MAC protocol is reader initiated. The Gen 2 MAC protocol is based on framed slotted ALOHA. Each frame, or *query round*, has a number of slots and tags reply in a randomly selected slot per frame.[3] A *query* command is then transmitted which specifies the uplink data encoding and number of slots for the subsequent backscatter modulation for uplink. The *query* command contains the Q parameter value (0–15) that allows a tag to choose a random slot between $(0, 2^Q - 1)$ in which to reply. The tag counter counts down to zero, and tag replies with a random 16-bit number (*RN16*); two (or more) tags that choose the same back-off will thus collide. After receiving a successful *RN16* the reader responds with an ACK (which includes the *RN16*), in effect reserving that slot for the tag to backscatter its ID.

1) Tag Collision Resolution: As is clear, the uplink (read) rate is collision limited. Anticollision in Gen 2 framed ALOHA [20] is achieved via dynamic adjustment of the uplink frame size in every round (by the reader changing the Q value). Such methods rely on timely feedback from the reader based on the outcomes of prior transmission attempts (number of successful, collision, or idle slots) in the prior round(s). Since the number of tags involved in a collision event significantly affects performance, *Bayesian* approaches based on side information such as the estimated unread tag population as in [20] and [21] are promising. Nonetheless, irrespective of the dynamic frame size adjustments, the maximal efficiency is still bounded by 0.367 of slotted random ALOHA. Clearly, anticollision approaches based on tree walking are more promising, since it is well known that the maximum utilization of binary depth first search with m-ary splitting multiple access (DMSA) is 0.43. However, this

[3]The reader can optionally transmit a *select* command first which limits the number of tags that respond in the round.

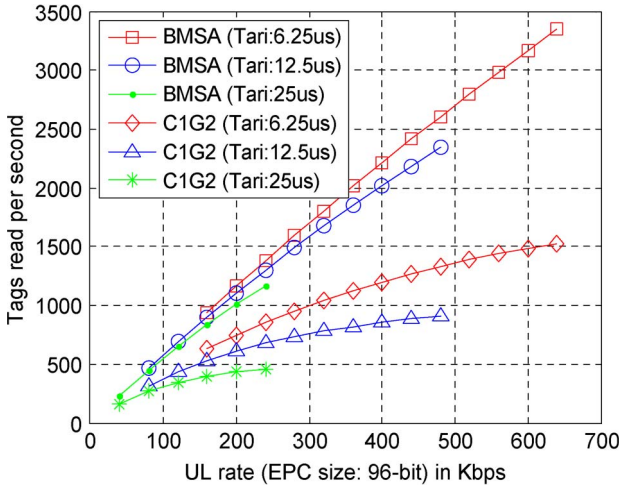

Fig. 2. ***Enhancement in tag read rates via hybrid (BMSA) anticollision [18].***

requires the tags to listen to slot-based reader feedback Accordingly, some recent work has focussed on suitable *hybrid* schemes that utilize breadth-first search with *m*-ary splitting (BMSA) [18]. The contention resolution algorithm is characterized by a *variable* splitting factor *m*. Collision resolution via BMSA can be embedded within the framed ALOHA protocol by assuming that the reader broadcasts the result of *each RN16 uplink slot access in the previous frame*. Contention resolution is managed more effectively by limiting the collided tags to contend only within their mutually exclusive subgroups, resulting from smart splitting choices determined by the reader. The resulting performance improvement in terms of tag read rate is shown in Fig. 2 and can be attributed to the following primary reasons: 1) reduction of downlink duration by eliminating frequent reader commands and corresponding guard space times during a session, and 2) improved uplink throughput via dynamic choice of the splitting factor *m* as a result of the slot-by-slot outcome information from the previous frame.

III. TOWARDS AN RFID SENSOR NET

We now describe two innovations by our group that we believe constitutes significant milestones in evolution of RFID technology: 1) the WISP tag [12] that integrates sensing functionality while preserving low-power operation and enhancing programmability and 2) software-defined reader [16] that provides researchers with much needed lower layer controls to investigate the impact of various optimization approaches described at the link and MAC layers in the earlier sections. Currently, the WISPs are being made available to sensor networking research community to further promote RFID-based networking.[4]

[4]The WISP hardware and associated software will be distributed to academic researchers via the WISP challenge program under a BSD open source license; see http://www.seattle.intel-research.net/wisp.

A. A New Passive RFID Tag: The WISP

The WISP is an augmented tag, powered and read by the commercial off the shelf EPC Gen 2 RFID readers. Unlike conventional tags, WISPs include a fully programmable, low-power microcontroller unit (MCU) and sensors. The cornerstone of low-power operation rests on enhanced power harvesting and capacitive storage as well as envisaged future enhancements—via integrated circuit and MAC optimization—to the overall link and protocol stack. The EPC Gen 2 protocol is implemented in software on the microcontroller instead of a dedicated hardware finite state machine; this enhanced programmability is expected to be a critical component enabling future RFID system optimization.

A block diagram of the WISP is shown in Fig. 3; the analog block consists of a demodulator, a regulator, and a voltage supervisor. The regulator and the voltage supervisor are always on and consume approximately 2 μA. The demodulator is enabled by the MSP430 microcontroller (MCU) when there is sufficient energy accumulated in the storage capacitor as indicated by the voltage supervisor. The demodulator draws approximately 10 μA, which is dominated by an analog comparator with <1-μs propagation delay. This allows detection of the reader-to-tag modulation. The RF block includes a rectifier for converting RF energy into dc power and a modulator for controlling the reflection coefficient between the antenna and the tag. The modulator has no static power consumption, however, when the modulator is reflecting power from the tag, there is a loss of available power to the tag. The rectifier has significant static leakage of approximately 15 μA. However, a low-leakage Schottky diode placed between the rectifier and the storage capacitor limits current from flowing back through the rectifier. The rectified voltage is connected to a regulator and two voltage supervisory circuits. The microcontroller's nominal operating voltage is 1.8 V, but it can retain the contents of RAM down to 1.6 V. If the 1.6-V supervisor detects a voltage less than 1.6 V, it causes a hard reset of the microcontroller. When the voltage is within 1.6–1.9 V, the microcontroller enters a very low-power RAM retention only mode.

The protocol block is defined in software through the MCU. The MCU power consumption is approximately 200 μA/MHz and draws only 0.1 μA in sleep mode. WISP is able to detect the start of a communication packet without enabling the demodulator or RX MCU mode, which enables very low quiescent current consumption. RX requires a 4-MHz clock rate (800 μA) while TX requires a 2-MHz clock rate (400 μA). The clock rate is driven by the modulation type, where faster modulations require a higher clock rate. RX requires a higher clock rate than TX because it performs clock and data recovery, while the TX relies on a calibrated internal clock for TX modulation. The MCU includes an on-chip 10-bit ADC with 4-μs conversion time and 500-μA current consumption. Packet construction, including 16-bit CRC, thus

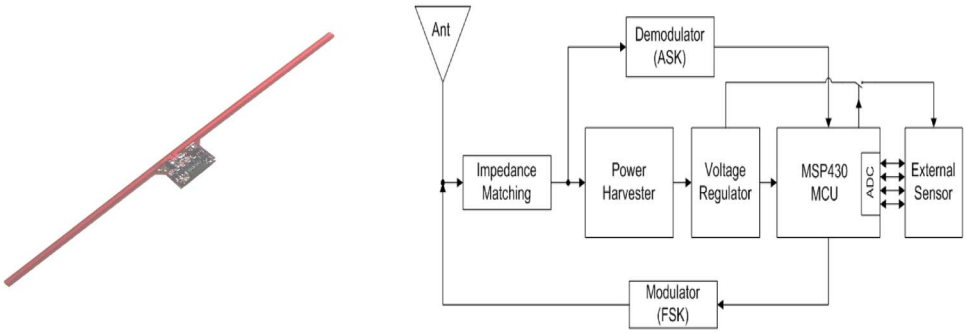

Fig. 3. ***WISP picture and schematic.***

requires roughly 200 μs at 4-MHz clock rate. Sensor power consumption varies widely, ranging from 7.5 μA for a temperature sensor (MAX6613) to 180 μA for a three-axis accelerometer (ADXL330). Sensors are preferably disabled when not in use to minimize power consumption. However, analog filtering requirements necessitate some settling time between enabling the sensor and analog-to-digital conversion. This is relatively costly for sensors such as the accelerometer which require several milliseconds of settling.

The flexibility and programmability of WISP has enabled application to a variety of applications. Sensors that have been interfaced to the WISP include light, temperature, acceleration, and strain [12]. Adding a supercapacitor to the WISP, we have created a wirelessly rechargeable data logger that can read and log temperature and fluid level data for 24 hours without physical proximity to an RFID reader. When the tag is brought near a reader, it reports back the logged data and wirelessly recharges the supercapacitor [14].

There are several design considerations underlying an optimized ASIC tag design. First, the analog components including bias generation, voltage regulation, and demodulation must be chosen for robust performance and low quiescent current under wide variations in supply voltage. The digital logic should minimize switching activity, especially in idle mode, through clock gating and clock rate scaling. Finally, the RF-to-dc converter must be optimized for maximum RF sensitivity under the operating load of the tag.

Sensing applications present new challenges for tag designers. Signal conditioning amplifiers must be low noise in order to detect microvolt signals but also maintain low power consumption for long range and high throughput. To obviate the need for constant signal digitization, low-power analog event detection circuits can wake the digital core upon an event. This allows digitization, characterization, logging, and communication to be performed only while the signal of interest is present. Performing complex computational tasks such as data processing requires continued innovation. For example, WISP has been employed to test a check-pointed computational scheme where processing results are saved to nonvolatile memory when tag power is not available [15].

B. The Software-Defined Reader

We have also developed a new software-defined Gen 2 RFID transceiver that can communicate with commercial tags while giving researchers greater control over the physical and MAC layers of the protocol [16]. The reader design is based on COTS components—notably the Universal Software Radio Peripheral (USRP) and the GNU Radio signal processing toolkit [22]. The USRP is a low-cost, general purpose RF front end for software radio development that interfaces with a standard PC via USB, with nearly all signal processing being performed on the host using GNU Radio software.

The USRP motherboard receives data via four ADCs operating at 64 Msps and outputs via a USB 2.0 interface to the host computer. Daughterboards downconvert RF signals (e.g., 900 MHz) to the IF range on the motherboard ADCs. Each USRP motherboard is equipped with two daughterboards to allow simultaneous txmit-receive. The USB interface to the host acts as the bandwidth limiter, with a maximum delivery rate of 8 Msps; hence subsampling (and interpolation) is needed between the USRP data path and the USB. Thus, the flexibility of the USRP and GNU Radio comes at the cost of transceiver latency.

The configuration parameters for our architecture fall into three categories—USRP configuration, Gen 2 protocol parameters, and GNU Radio block parameters. USRP configuration consists solely of setting the frequency in the range of 902–928 MHz. All Gen 2 MAC parameters can be configured, such as the number of slots in the frame and the uplink encoding. The downlink and uplink rates in Gen 2 are determined by the pulse widths used during the preamble that precedes the *query* command that are exposed as configuration options. Based on the uplink PHY parameters, the pulse width for the matched filter is set, along with the filter decimation in order to provide two samples per symbol as required by the clock recovery block.

The complete Gen 2 MAC protocol was implemented. We encountered three major challenges: 1) high latency, 2) imprecise timing, and 3) the low transmit power of the USRP daughterboard. Performing signal processing in software at the host greatly increases system latency compared to conventional hardware transceivers. Specifically, the platform incurs the latency cost of the low rate USB interface, a series of buffers in the receive and transmit chains, and the fact that the GNU Radio software is running on a general purpose computer on top of an OS. Previous work using the USRP and GNU Radio has shown transceiver latency on the order of tens of milliseconds, far too high for implementing most wireless MAC protocols.

Because the Gen 2 protocol is designed for use with very low cost tags and low rate uplink, the timing requirements of the MAC are relaxed compared to most protocols. Depending on the system configuration, the maximum time in which an ACK must be sent can be as high as 500 μs. While this is much higher than required by other wireless protocols, it is two orders of magnitude less than the tens of milliseconds achieved by prior implementations. Consequently, reliably meeting the timing requirements of commercial tags was the major challenge to implementing our transceiver.

IV. CONCLUSION

RFID sensor nets will require advances on multiple fronts pertaining to components as well as protocols. These include, notably, new tag designs inclusive of sensor integration, enhancements to link (modulation and coding on transmit and receive signal chain) and multiaccess layers as well as fundamental innovations towards an overall power management strategy. In this work, we have highlighted some progress on several of these fronts and indicated future directions for research and innovation for the RFID-based sensor networking community. ■

REFERENCES

[1] "Draft protocol specification for a class 1 radio frequency identification tag," Auto-D Center, Cambridge, MA, 2003.

[2] EPC, Radio-frequency identity protocols class-1 generation-2 UHF RFID protocol for communications at 860 MHz–960 MHz version 1.0.9, Jan. 2004.

[3] D. Dobkin, *The RF in RFID: Passive UHF RFID in Practice*. New York: Elsevier, 2008.

[4] R. Glidden, C. Bockorick, S. Cooper, C. Diorio, D. Dressler, V. Gutnik, C. Hagen, D. Hara, T. Hass, T. Humes, J. Hyde, R. Oliver, O. Onen, A. Pesavento, K. Sundstrom, and M. Thomas, "Design of ultra-low-cost UHF RFID tags for supply chain applications," *IEEE Commun. Mag.*, vol. 42, no. 8, pp. 140–151, Aug. 2004.

[5] Why METRO's item level RFID deployment matters, Sep. 2007. [Online]. Available: http://www.rfidupdate.com/articles/index.php?id=1451

[6] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder with 16.7 μW minimum RF input power," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1602–1608, Oct. 2003.

[7] Texas Instruments, Active Mode Supply Current (Into VCC) Excluding External Current, Dallas, TX, Feb. 2009, MSP430F2132 datasheet.

[8] K. V. S. Rao, P. V. Nikitin, and S. F. Lam, "Antenna design for UHF RFID tags: A review and a practical application," *IEEE Trans. Antennas Propag.*, vol. 53, no. 12, pp. 3870–3876, Dec. 2005.

[9] G. D. Vita and G. Iannacone, "Design criteria for RF section of UHF and microwave passive RFID transponder," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2978–2990, Sep. 2005.

[10] R. Chakraborty, S. Roy, and V. Jandhyala, "Revisiting RFID link budgets for technology scaling: Range maximization of RFID tags," in *IEEE Trans. Microw. Theory Tech.*, 2010 (to appear).

[11] A. Sample, D. J. Yeager, P. S. Powledge, A. V. Mamishev, and J. R. Smith, "Design of an RFID based battery free programmable sensing platform," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 6, pp. 2608–2615, Nov. 2008.

[12] D. J. Yeager, Sample, and J. R. Smith, "WISP: A passively powered UHF RFID tag with sensing and computation," in *RFID Handbook: Applications, Technology, Security, and Privacy*, S. A. Ahson and M. Ilyas, Eds. Boca Raton, FL: CRC Press, 2008, pp. 261–276.

[13] J.-P. Curty, N. Joehl, C. Dehollain, and M.J. Declercq, "Remotely powered addressable UHF RFID integrated system," *IEEE J. Solid State Circuits*, vol. 40, no. 11, pp. 2193–2202, Nov. 2005.

[14] D. Yeager, P. Powledge, R. Prasad, D. Wetherall, and J. Smith, "Wirelessly-charged UHF tags for sensor data collection," in *Proc. IEEE Int. Conf. RFID*, Apr. 16–17, 2008, pp. 320–327.

[15] B. Ransford *et al.*, "Getting things done on computational RFIDs with energy-aware checkpointing and voltage-aware scheduling," in *Proc. USENIX Workshop Power Aware Comput. Syst.*, Dec. 2008.

[16] M. Buettner and D. J. Weatherall, "A flexible software radio transceiver for UHF RFID experimentation," UW-CSE Tech. Rep. #09-01-02, 2009.

[17] D. R. Hush and C. Wood, "Analysis of tree algorithms for RFID arbitration," in *Proc. IEEE Int. Symp. Inf. Theory*, 1998, DOI: 10.1109/ISIT.1998.708695.

[18] Y.-C. Ko, S. Roy, J. R. Smith, H.-W. Lee, and C.-H. Cho, "An enhanced RFID multiple access protocol for fast inventory," in *Proc. IEEE Global Telecommun. Conf.*, 2007, pp. 4575–4579.

[19] Y.-C. Ko, S. Roy, J. R. Smith, H.-W. Lee, and C.-H. Cho, "RFID MAC performance evaluation based on ISO/IEC 18000-6 type C," *IEEE Commun. Lett.*, vol. 12, no. 6, pp. 426–428, Jun. 2008.

[20] F. C. Schoute, "Dynamic frame length ALOHA," *IEEE Trans. Commun.*, vol. COM-31, no. 4, pp. 565–568, Apr. 1983.

[21] M. Kodialam and T. Nandagopal, "Fast and reliable estimation schemes in RFID systems," in *Proc. ACM Int. Conf. Mobile Comput. Netw.*, Sep. 2006, pp. 322–333.

[22] "GNU radio and USRP," Ettus Research, Mountain View, CA. [Online]. Available: www.ettus.com

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